EE143 – Fall 2016
Microfabrication Technologies

Lecture 12: Process Integration
Reading: Jaeger, Chap. 9

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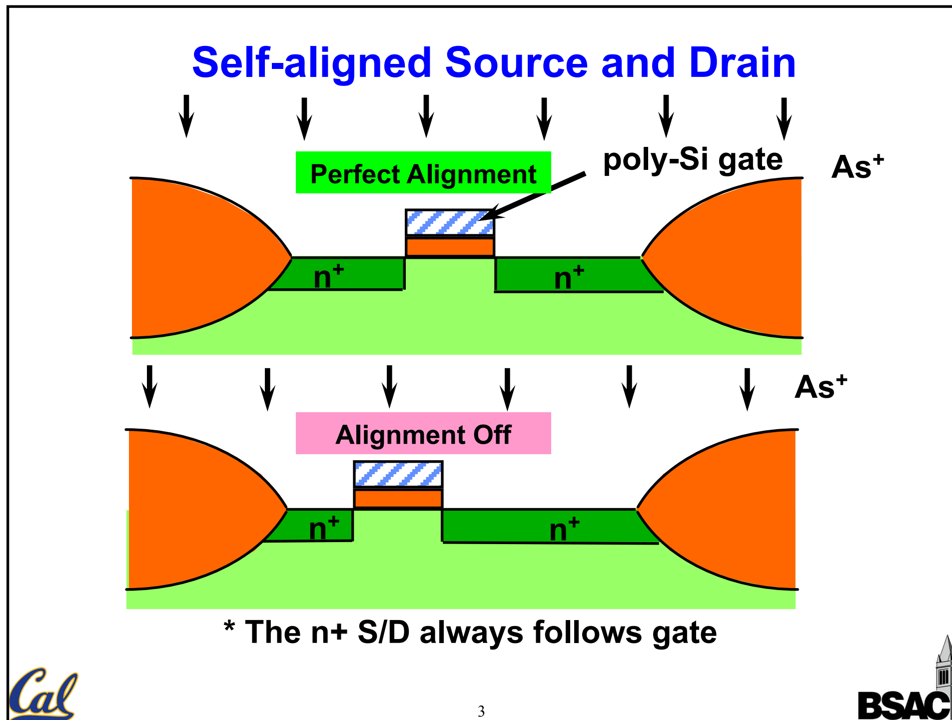
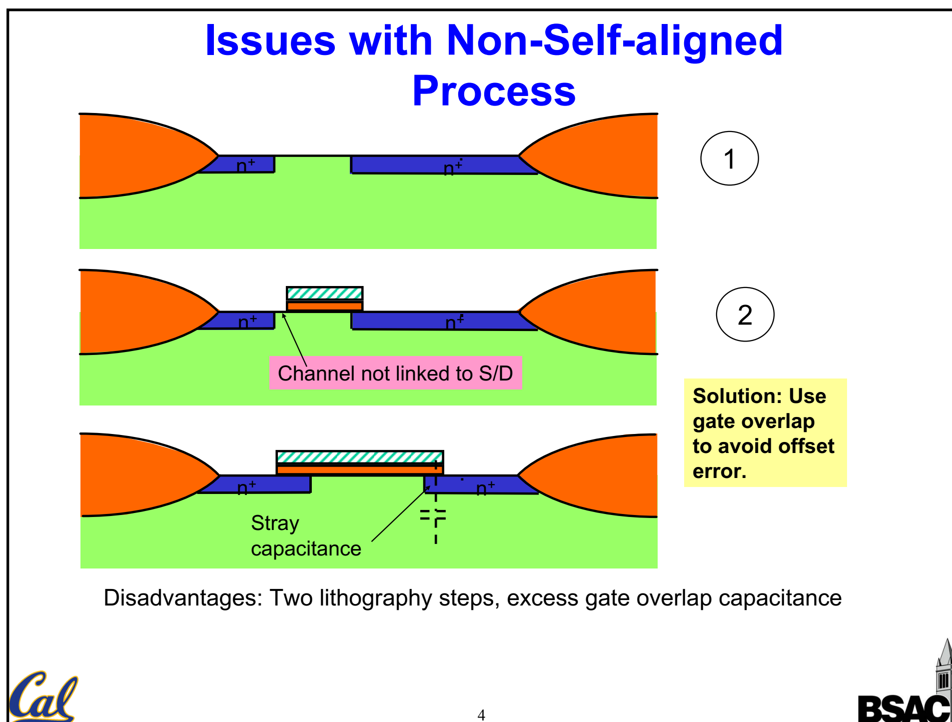
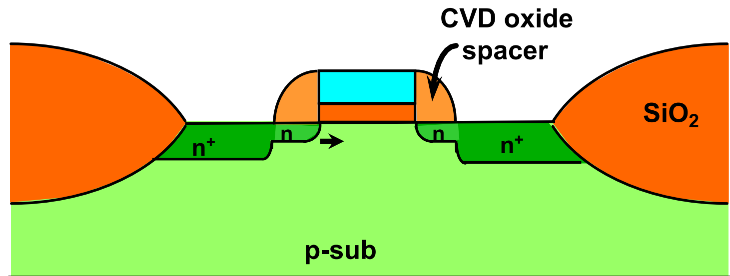
Process Integration

- Self-aligned processes
  - LOCOS- self-aligned channel stop
  - Self-aligned Source/Drain
  - Lightly Doped Drain (LDD)
  - Self-aligned silicide (SALICIDE)
- Example IC Process Flows
  - NMOS - Generic NMOS Process Flow
  - CMOS - The MOSIS Process Flow
- Advance MOS Techniques
  - Twin Well CMOS , Retrograde Wells , SOI CMOS


Self-aligned Source and Drain
Perfect Alignment
poly-Si gate
As+
n+
n+
As+
Alignment Off
n+
n+
* The n+ S/D always follows gate
3

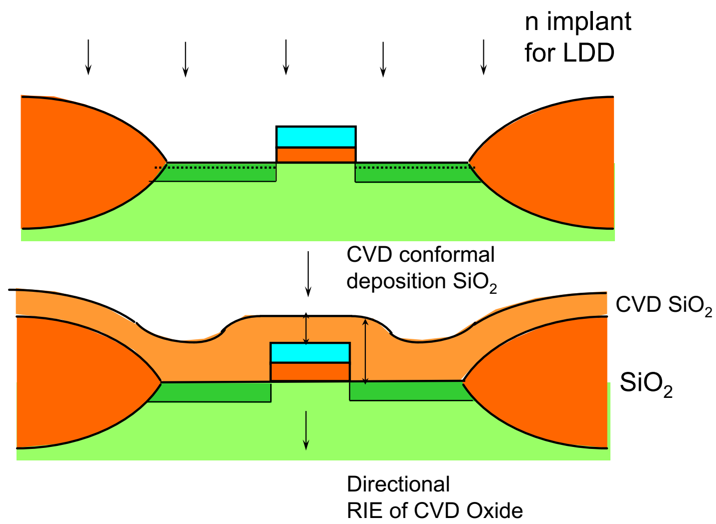

Issues with Non-Self-aligned Process
1
2
Channel not linked to S/D
Solution: Use gate overlap to avoid offset error.
Stray capacitance
Disadvantages: Two lithography steps, excess gate overlap capacitance
4

Lightly Doped Source/Drain MOSFET

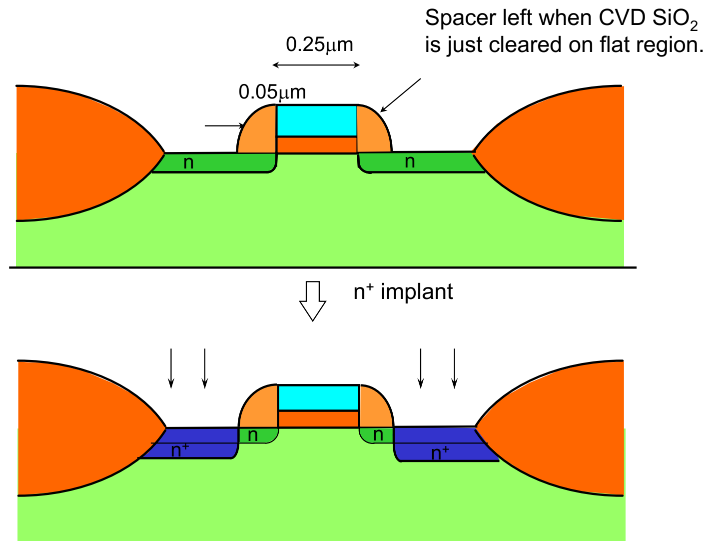


The n-pockets (LDD) doped to medium conc (~1E18) are used to smear out the strong E-field between the channel and heavily doped n+ S/D, in order to reduce hot-carrier generation.

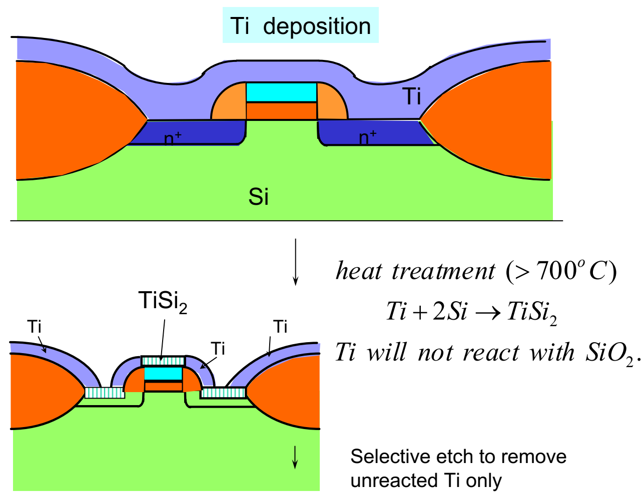
LDD Process



LDD Process (cont'd)



Salicide Integration



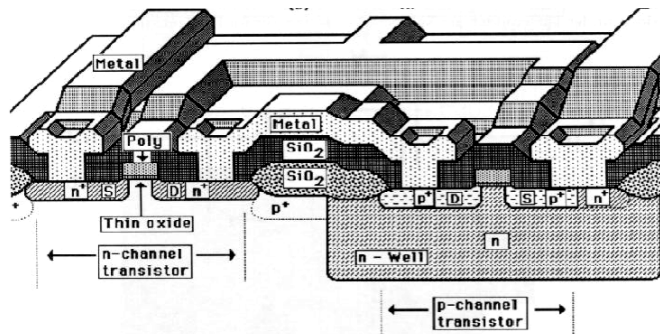
$heat\ treatment\ (> 700^o C)$

$Ti + 2Si \rightarrow TiSi_2$

$Ti\ will\ not\ react\ with\ SiO_2.$

Selective etch to remove unreacted Ti only

CMOS: Basic single-well process

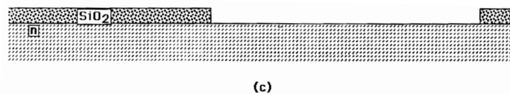


N-well CMOS structure

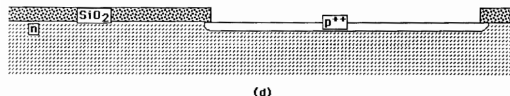
How many masks?
Process flow?

Single-well process (cont'd)

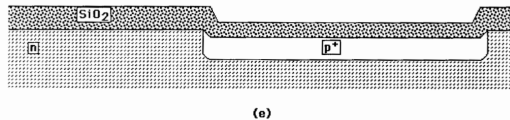
Pattern mask opening For p-well implant



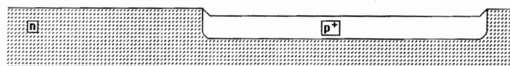
Shallow implantation of boron



Diffusion drive-in To form p-well in oxidizing ambient

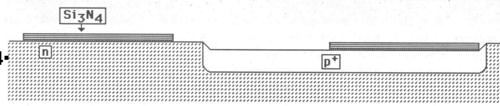


Remove masking oxide

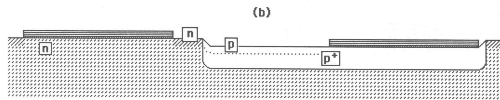


Single-well process (cont'd)

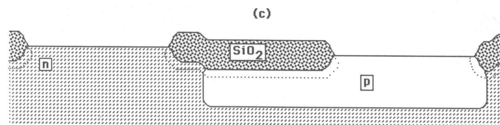
Pad oxide growth and CVD Si_3N_4. Pattern field oxide regions



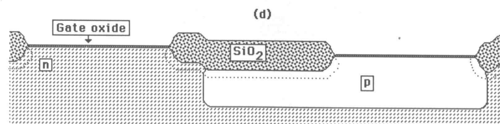
Blanket implant of Boron for p channel stop inside p-well Protect p-well regions with photoresist.



LOCOS Oxidation



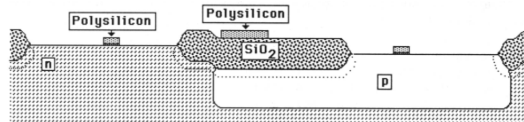
Thermal oxidation of gate SiO_2



Single-well process (cont'd)

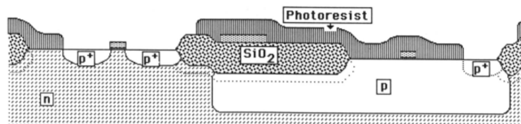
CVD poly-Si

Pattern poly-Si gates



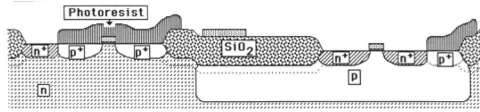
Protect ALL n-channel transistors with photoresist.

Boron implantation to form source/drain of p-channel transistors and contacts to p-well

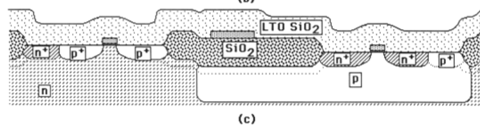


Single-well process (cont'd)

Protect ALL p-channel transistors with photoresist.

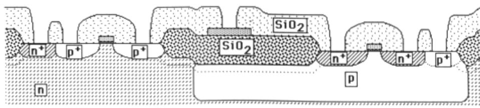


Arsenic implantation to form source/drain of n-channel transistors and contacts to n-substrate



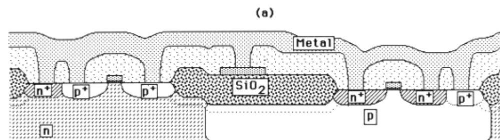
CVD SiO_2 (Low-temperature oxide)

Pattern and etch contact openings to source/drain, well contact, and substrate contact.

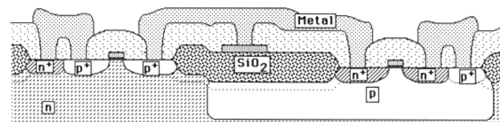


Single-well process (cont'd)

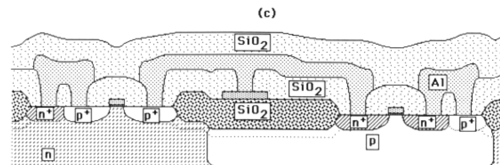
Metal 1 deposition



Pattern and etch Metal 1 interconnects

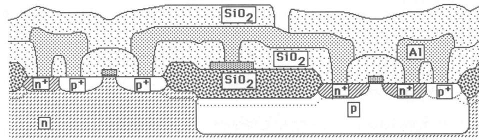


CVD SiO_2



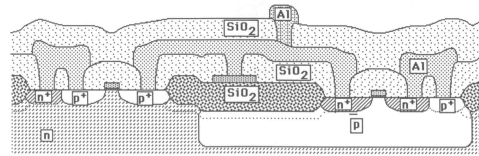
Single-well process (cont'd)

Pattern and etch contact openings to Metal 1.



Metal 2 deposition.

Pattern, and etch Metal 2 interconnects.



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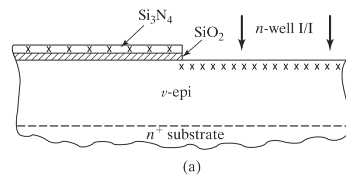
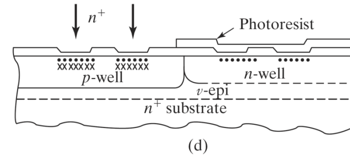
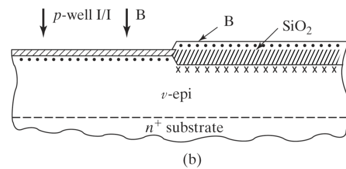
Twin-well CMOS Technology



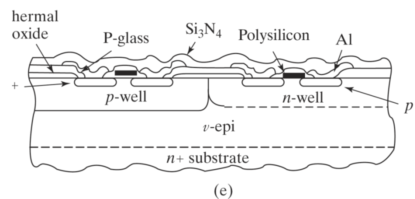
(a)



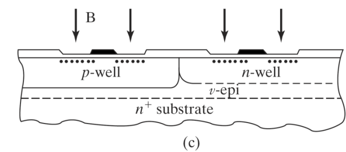
(d)



(b)



(e)



(c)

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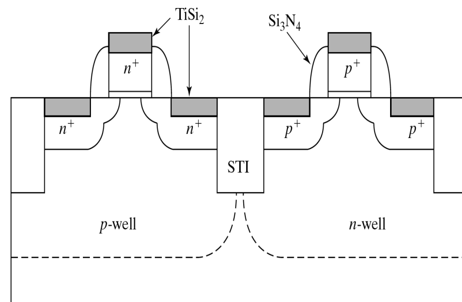
Shallow Trench Isolation



- Shallow trench isolation in a twin-well process
- Intercepts depletion layers permitting tighter spacing
- Reduces the chance of latchup